Overvoltage Protection for CMOS Switches and Multiplexers

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CMOS analog switches and multiplexers are critical components in many electronic systems. Even though their ruggedness and reliability have been demonstrated in countless applications, it is still not uncommon to encounter “mysterious” failures caused by conditions that exceeded the absolute maximum ratings. By including overvoltage and fault protection in your circuits, you can achieve successful designs that will be in service for many years and will provide better performance at a low cost.

Identifying The Problem

Overvoltage (OV) refers to a case where the analog signal amplitude applied to a switch terminal exceeds the power supply rails. A fault can also occur when power to a CMOS device is lost while the analog signals are still on.

From the simplified CMOS switch cross section shown in Figure 1, it is obvious that if voltages outside the power supply rails are applied to the source or the drain, or if power to the chip is lost, one or more of the parasitic diodes (D1 through D4) will become forward biased. Therefore, it is necessary to take precautions so that the power dissipation capabilities of these diodes are not exceeded, otherwise unprotected devices can malfunction or be destroyed.

This application note refers mostly to the DG408 (8-channel multiplexer), but the same principles apply to most CMOS analog switches and multiplexers.

Fault Currents

When the diodes shown in Figure 1 are allowed to conduct, as during an overvoltage condition, potentially damaging currents can occur. Additionally, the analog signal gets clamped to the supply rail, which can overload the signal source and produce signal clipping. This condition may be detrimental if the analog signal is also going to another destination.

In the circuit shown in Figure 2, per Ohm’s law, the current flow is limited only by the generator’s resistance (R_g) and by the the forward biased diode’s resistance (R_d). At 25°C, R_d may have values that range from 6 Ω (DG408) to 19 Ω (DG508A). Therefore the fault current is given by

$$i_f = \frac{V_g - (V+) - V_F}{R_g + R_d}$$

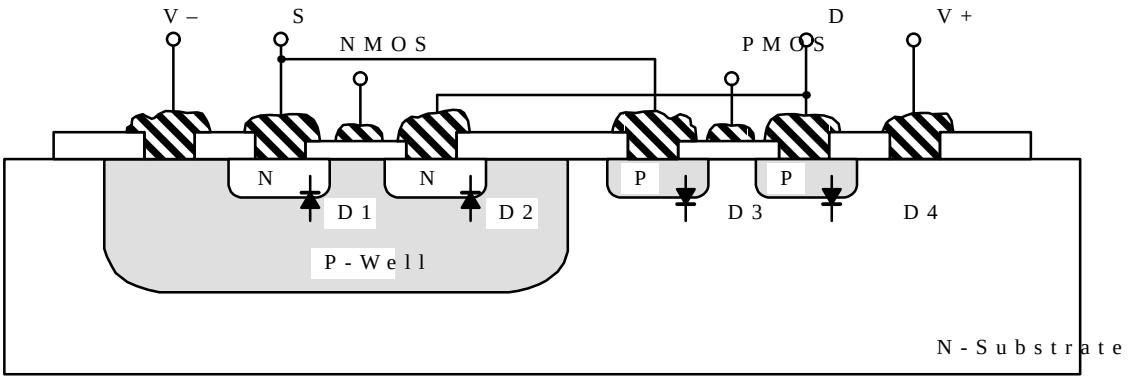

Figure 1. CMOS Switch Cross Section Showing Parasitic P-N Junctions

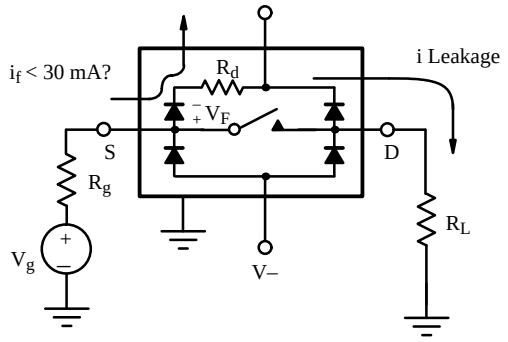

Figure 2. Fault Current Flows When V_g > V+

As long as i_f does not exceed the absolute maximum continuous-current rating (source or drain, typically 20 or 30 mA) no problem will occur. For instance, when using the 8-channel silicon-gate multiplexer (DG408) in an audio system where R_g = 600 Ω, V_g will have to exceed V+ by more than 12 V before it reaches the 20-mA limit.

On the other hand, a 12-V overvoltage coming from a 1-Ω signal source will produce 1.6 A. At that current, it won't take long for the device to be damaged. A similar situation occurs for negative overvoltages. Due to the rectifiers used in most power supplies, a supply will not sink current if it was designed to source it. That is, if V+ is supposed to be +15 V and V_g is equal to +20 V, do not be surprised if V+ loses regulation and rises to one diode drop below V_g. V_g ends up supplying power to the whole circuit, and the question becomes whether or not the additional voltage will exceed the ratings of the other components in the circuit.

Crosstalk And Latchup

Ideally, when one channel experiences an overvoltage condition, processing the information arriving on the other channels would still be possible. But since the clamping diodes are part of parasitic transistors (Figure 3), when activated, they can induce leakage currents on other channels located on the same chip. This condition is especially inconvenient when dealing with CMOS multiplexers. The channel experiencing overvoltage will cause dc offsets (sometimes called crosstalk) on the output even when one of the good channels is selected. This form of crosstalk or error source is demonstrated by the test circuit shown in Figure 4. Figure 5 is the resulting scope plot. Note that when S1 is supposed to be off and S8 is on, every time the analog signal rises above V+, the output shows a positive voltage signal instead of zero. When S1 is turned on, the output shows considerable distortion because the signal is clamped to the +8-V rail.

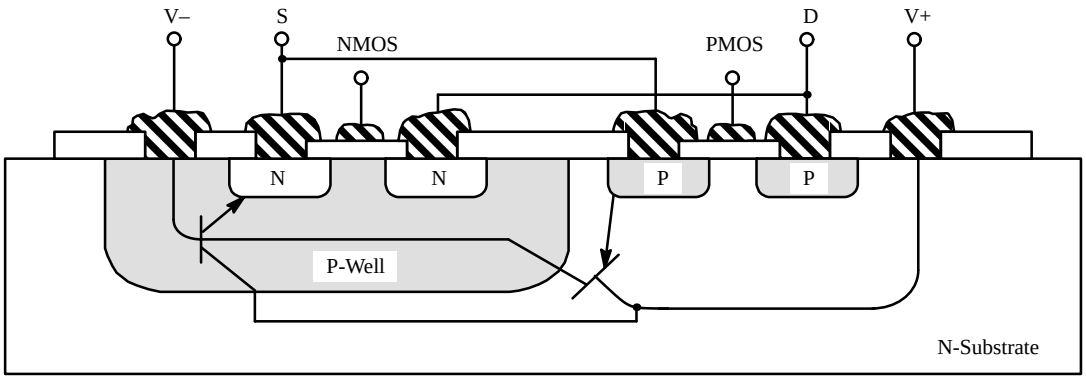

Figure 3. Two Parasitic Transistors Form an Intrinsic SCR on a CMOS structure

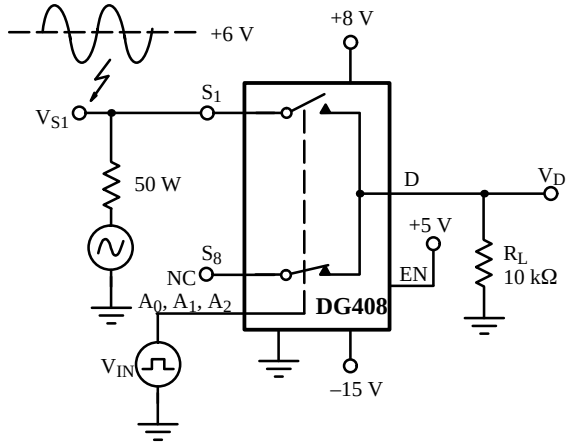

Figure 4. Test Circuit Used to Evaluate OV Induced Crosstalk

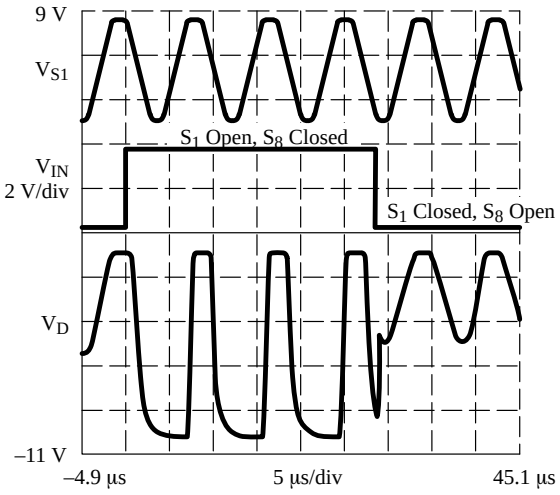

Figure 5. Scope Plot of the Test Circuit Shown in Figure 4

If the combined gain of the two parasitic transistors shown in Figure 3 is more than 1, a real SCR results. It can be triggered by a very small fault current. The condition is known as latchup, and the effect is a loss of switch control. No matter what the logic input is, the switch will remain unresponsive until both the overvoltage and the power are removed from the device. Without current limiting, latchup can cause permanent damage to the chip. This phenomenon plagued many early CMOS switches. With advances in design techniques, such as the use of buried layers (to reduce transistor gain) and isolated polysilicon resistors (for current limiting), all Siliconix CMOS switches are self-resetting—that is, latchproof.

The Solution: Overvoltage Protection

The two main objectives are

1. To protect the analog switch or multiplexer from suffering physical destruction due to fault currents
2. To avoid degradation of the analog signals in the system due to overloads, signal clipping, and crosstalk problems.

The most popular protection methods use one or more of the following:

- Reverse-current blocking diodes
- Current limiting
- Picoamp diode clamps.
- Reverse-Current Blocking Diodes

A convenient and inexpensive form of overvoltage protection consists of adding two small diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 6).

During an OV condition, this arrangement protects the multiplexer and the signal source by blocking the flow of reverse current via the substrate diodes. It floats the supply pins above or below the normal V– or V+ rail. In this case,

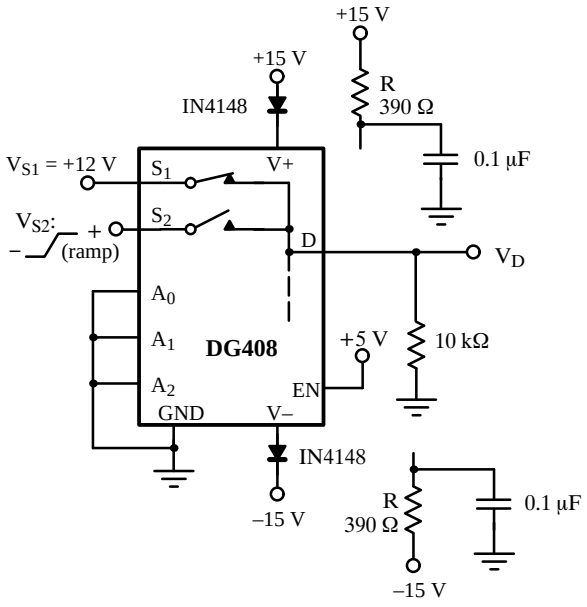

Figure 6. Overvoltage Test Circuit

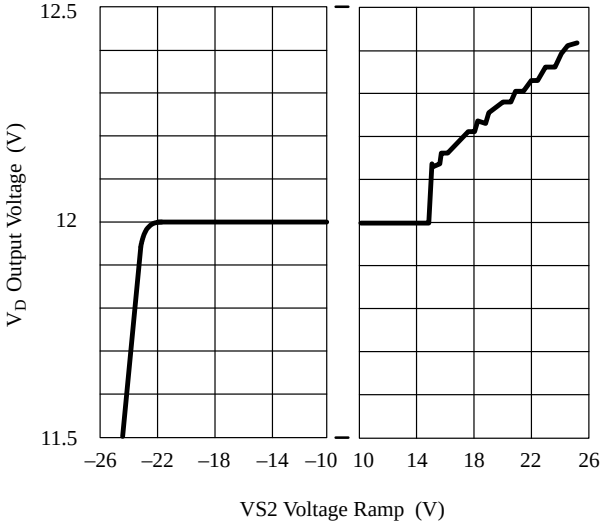

Figure 7. Overvoltage-Induced Errors for the Diode-Protected Circuit of Figure 6

the OV signal actually becomes the power supply to the IC. Damage to the chip is avoided as long as the difference, Vg – (V–), does not exceed the absolute maximum breakdown voltage limit for the process (44 V). The addition of these diodes reduces the analog signal range by two diode drops [to (V–)+ 0.7 V minimum and (V+) – 0.7 V maximum], but it preserves the low channel resistance and low-leakage characteristics so that the error term, $r_{DS(on)}$ x $I_{D(on)}$, is kept to a minimum.

This method does not eliminate crosstalk or leakage to other channels. The test circuit shown in Figure 6 illustrates what happens. Here +12 V dc was applied to a 10 kΩ load via channel one of the multiplexer. At the same time, a ramping dc voltage (V_{S2}) was applied to the adjacent channel (S2). The output voltage V_D was then plotted as a function of V_{S2}. Figure 7a shows that the output voltage develops an error as soon as V_{S2} goes above +15 V. In the negative direction, however, the error only becomes significant when V_{S2} reaches –21 V (see Figure 7).

Current Limiting Resistors

Protection of analog multiplexers can also be accomplished by installing current-limiting resistors in series with the power supply leads. This is shown on Figure 6 where the R-C networks are installed in place of the 1N4148 diodes. During normal operation, the bypass capacitors provide the current pulses required when the analog multiplexer changes states. During a fault condition the reverse current is given by

$$i_f = \frac{V_g - (V+) - V_F}{R_g + R_d + R}$$

From this expression, the required value of R can be calculated. For example, if 28 V dc (0-Ω source impedance) is connected to one of the source pins and the operating supplies are ¿15 V, the minimum value of R needed to protect a DG408 is given by

$$R = \frac{28\ V - 15\ V - 0.7\ V}{30\ mA} - 6\ \Omega = 404\ \Omega$$

(The diode resistance, R_d, is assumed to be 6 Ω)

An advantage of the current-limiting resistor method is that the R-C networks help to eliminate any switching noise that would otherwise appear on the analog power supply lines every time the multiplexer changed states.

A disadvantage is that the errors seen on a good channel when an adjacent channel experiences an overvoltage are greater than those resulting when reverse-current blocking diodes are used (see Figure 8).

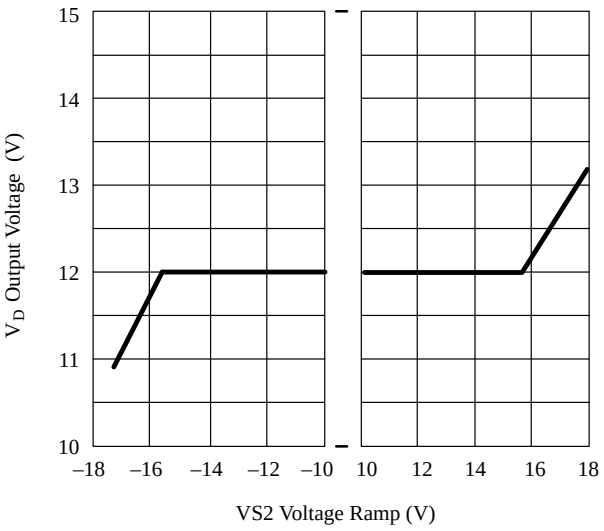

Figure 8. Overvoltage-Induced Errors for the Resistor-Protected Circuit of Figure 6

Picoamp Diode Clamps

Figure 9 shows a multiplexer overvoltage protection method that uses external picoamp diodes to divert the fault current away from the internal clamping diodes. Siliconix' picoamp diodes (PADs) provide a superior alternative to conventional diodes since they practically

eliminate reverse-current (leakage) induced errors. Reverse-current specifications under one picoamp are possible (PAD1).

Forward current through the PADs should be limited to 50 mA, so a series current limiting resistor (R_1) may be required. For more information, consult the JPAD/PAD/SSTPAD data sheet.

The PAD protection method preserves system accuracy and speed at the expense of a large number of external protection components. The clamping voltages do not need to be accurate. They may be supplied by Zener references.

Fault Protected Multiplexers

To eliminate the need for external protection, several types of overvoltage and/or fault protected multiplexers have been designed. Some, like the HI-508A, use an internal 1-kΩ current-limiting resistor in series with each analog switch. The higher equivalent $r_{DS(on)}$ increases leakage-induced errors, slows down settling times and, under fault conditions, may cause excessive power dissipation.

Other designs like the MAX358 and the Siliconix DG458 use three MOSFETs in series (two n-channels and one p-channel) to form a self-protecting analog switch that turns itself off when the analog signal level approaches or exceeds the power supply voltage rails.

Figure 10 illustrates the equivalent circuit for one channel. This protection method reduces the analog signal range by approximately two volts from each power supply rail, increases charge injection-induced offset errors, and increases settling times due to the increased $r_{DS(on)}$.

Conclusion

No overvoltage protection method is perfect. Existing OV protected multiplexers are more expensive and sacrifice performance with their higher $r_{DS(on)}$, longer settling times, and higher charge injection. They are convenient and easy to design with if system accuracy is not critical. If your circuit design does not require remote signal generation, or if you must try to maintain the highest accuracy possible, then the standard unprotected analog switches and multiplexers with or without the external orvervoltage protection methods discussed in this application note should be used.

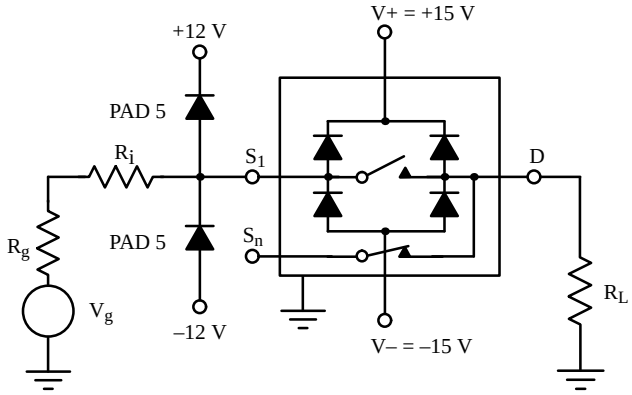

Figure 9. Pico-Amp Diode Clamps Used to Protect the Switch/Multiplexer and Preserve Accuracy on Remaining Channels

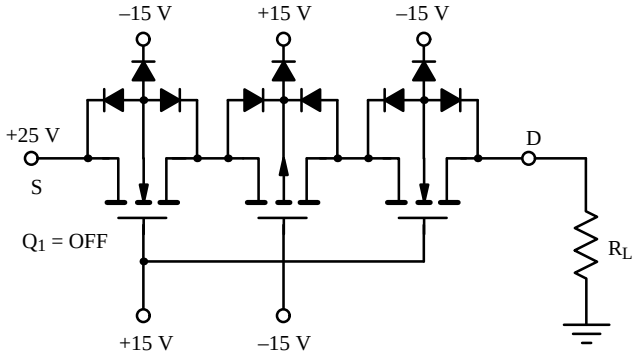

Figure 10. The 3-FETs-in-Series Channel Offers Inherent Fault Protection